Strain Compensated InGaAs/AlAs Triple Barrier Resonant Tunneling Structures for THz Applications

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***Abstract*—We report a theoretical study of InGaAs/AlAs triple barrier resonant tunneling heterostructures, which are optimized for operation in the terahertz frequency range, and compare these to current state-of-the-art double barrier structures reported in the literature. We consider the effect of strain introduced due to the large lattice mismatch between the substrate, quantum well, and potential barrier materials and describe designs with strain compensated active regions. Constraints have been imposed on the designs to minimize charge accumulation in the emitter quantum well, which is often associated with more complex triple barrier structures. The use of a triple barrier structure suppresses the off-resonance leakage current, thus increasing the maximum output power density, with $\approx$3 mWμm^{-2} predicted at 1 THz. The use of thinner potential barriers also reduces the carrier transit time through the structure, which increases the maximum output frequency, predicted to be $\geq$4 THz for optimized structures.**

***Index Terms*—Resonant tunneling diodes (RTDs).**

I. Introduction

THE frequency range from 300 GHz to 10 THz, typically known as the terahertz region of the electromagnetic spectrum is of great interest due to its potential applications. Enhanced security imaging [1], which exploits the unique "terahertz fingerprint" of many nonconducting materials to identify hidden objects, ultrafast wireless communications for short range high-capacity line of sight communication [2], and noninvasive highly sensitive medical imaging due to the nonionizing nature of the terahertz radiation [3] are a few of the potential applications offered by radiation in this frequency band.

Despite the development of several optical and electrical devices, which operate in the THz frequency range, the applications and commercial opportunities are still limited. Optical terahertz sources that have been developed are challenged by difficulties in obtaining suitably low energy band-to-band transitions and the need for cryogenic cooling to operate at THz frequencies [4], and as such are incompatible with compact modern electronic circuitry. Solid state sources, however, despite being compact, are limited in operating frequency by the carrier transit time, which is often too long for devices to operate in the THz frequency band [5]. Therefore, the lack of practical and coherent THz radiation sources has led to the term "terahertz gap" [6] being used to describe this frequency range.

Resonant tunneling diodes (RTDs) exploit the phenomenon of quantum mechanical tunneling, which is inherently a fast process, and unlike conventional electronic devices the operational speed of RTDs is mainly governed by the carrier tunneling time through the structure rather than a conventional transit time. Thus, RTDs are widely recognized as the fastest solid-state electronic devices.

Conventional double barrier RTDs, which are well studied, are used in current state-of-the-art devices [7]; however the most recent improvements in the measured emission frequency of these devices have been as a result of improved device fabrication and design, rather than improved structure design. Triple barrier RTDs are less studied and exhibit more complex resonant tunneling mechanisms [8]. These have been considered for their potential to operate at higher frequencies and with more output power than conventional double barrier structures [9]–[12].

The addition of a third potential barrier is essential to reduce the background leakage current, which dominates the off-resonance valley current in double barrier structures, whilst maintaining the high transmission coefficient through the device, which contributes to a large on-resonance current. This in turn improves the difference in the peak to valley current ΔI, which is an important device parameter for both maximum output power and frequency of oscillation.

To achieve oscillation frequencies in the THz window with sufficient output power to be utilized in real-world applications, an optimized double barrier resonant tunneling structure has been developed in the $In_{0.53}Ga_{0.47}As$/AlAs (indium gallium arsenide/aluminum arsenide) material system grown on lattice matched InP (indium phosphide) and reported by Kanaya *et al.* [13], and similar structures are currently being utilized in state-of-the-art RTDs, which have recently been reported operating with a frequency of 1.92 THz [14] at room temperature.

Due to the increased degree of complexity of triple barrier RTDs a thorough understanding of the behavior of these structures is needed, along with careful consideration and optimization of the triple barrier design. A recent study optimizing a triple barrier structure in the GaAs/AlGaAs material system has been

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reported [15]; however high-frequency operation of devices in this material system are less practical for general exploitation due to the required low temperatures.

In this paper, we report a theoretical optimization study of triple barrier RTDs, which build on the current state-of-the-art double barrier designs, whilst still considering the practical growth requirements for strain compensation of the InGaAs/AlAs material system.

II. Requirements for THz Emission

The negative differential conductance regions exhibited in the current–voltage (*I–V*) characteristics of resonant tunneling devices, combined with an appropriate resonant circuit allow for emission of high-frequency radiation, which can extend into the THz frequency regime. The theoretical maximum oscillation frequency of an RTD (f_{MAX}) has been known for many years and is given by (1) [16] and based on the small-signal equivalent circuit of an RTD given by Brown *et al.* [17]

$$f_{\mathrm{MAX}} = \frac{1}{2\pi}\left(\frac{1}{2{L_{QW}}^2 C_{\mathrm{D}}}\right)^{\frac{1}{2}}\left\{2L_{QW} - \frac{C_{\mathrm{D}}}{G^2} + \left[\left(\frac{C_{\mathrm{D}}}{G^2} - 2L_{QW}\right)^2 - \frac{4{L_{QW}}^2(1+R_{\mathrm{S}}G)}{R_{\mathrm{S}}G}\right]^{\frac{1}{2}}\right\}^{\frac{1}{2}} \quad (1)$$

where C_{D} is the space charge capacitance resulting from the charging and discharging effect of charge carriers within the device depletion regions, G is the negative differential conductance, and R_{S} is the device series resistance, which includes contact resistance, spreading resistance, and the resistance of the emitter and collector regions. L_{QW} is known as the quantum inductance and is given by

$$L_{QW} = \frac{\tau_{\mathrm{rtd}}}{G} \quad (2)$$

where τ_{rtd} is the tunneling time through the RTD structure. In suitably designed structures, L_{QW} can be shown to not have a significant impact on the high-frequency operation of RTDs [18] and (1), to a good approximation, reduces to [19]

$$f_{\mathrm{MAX}} = \frac{1}{2\pi C_{\mathrm{D}}}\sqrt{\frac{G}{R_{\mathrm{S}}} - G^2}. \quad (3)$$

Thus, to maximize the device oscillation frequency, minimizing the passive device components such as the series resistance and parasitic capacitances, whilst maximizing the negative differential conductance is necessary, where the average negative differential conductance of a resonant peak in the device *I–V* characteristic can be calculated from [20]

$$G = \frac{3}{2}\frac{\Delta I}{\Delta V} \quad (4)$$

where ΔI is the peak to valley current difference and ΔV is the peak to valley voltage difference.

Whilst maximizing G is an important consideration in optimization of the maximum frequency of oscillation, for practical devices and for commercial applications of such devices, the maximum output power is important.

The maximum output power for resonant tunneling devices with a static *I–V* characteristic (in the steady state), which is represented by a cubic polynomial can be calculated [21], where

$$P_{\mathrm{MAX}} = \frac{3}{16}\Delta I \Delta V. \quad (5)$$

However, for practical applications it is more appropriate to consider the frequency-dependent output power, $P_{\mathrm{MAX}}(f)$ [22]

$$P_{\mathrm{MAX}}(f) = \frac{3}{16}\cos\left[\omega(f)\tau_T\right]\Delta I \Delta V. \quad (6)$$

The total intrinsic delay of the charge carriers traveling through the resonant tunneling structure τ_T serves to decrease the maximum output power with increasing frequency and is given by [23]

$$\tau_T = \tau_{\mathrm{rtd}} + \frac{\tau_{\mathrm{dep}}}{2} \quad (7)$$

where τ_{rtd} is the carrier tunneling time, and τ_{dep} the carrier transit time in the depletion region. This finite transit carrier time reduces the negative conductance with increasing frequency and thus for high power output at high frequency, a large negative differential conductance region (ΔI and ΔV) as well as a short device transit time is required.

With the ever increasing need for low power consumption devices it is also extremely important to consider the power efficiency of the RTDs. Since the output power of the device is related to the difference between the peak and valley voltages ΔV and not the magnitude of the applied voltage itself, to minimize the wasted power it is desirable for the current resonance peak to occur at a low voltage whilst maintaining a large current.

To analyze and compare the input to output power efficiency of these structures a figure of merit suggested by Baba *et al.* [24], which is the ratio of the time-averaged electrical chip power P_{Chip} to the steady-state extractable power P_{MAX} is used.

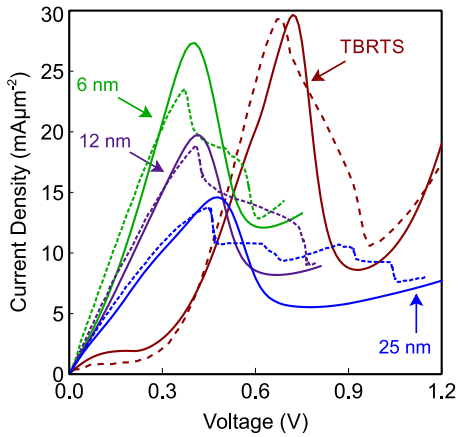

Fig. 1. Simulated (solid lines) and experimentally measured (dotted lines) current density against applied voltage for the structures from Kanaya *et al.* [13] and Sekiguchi *et al.* [30]. There is good agreement between the simulated and experimentally measured values for double barrier structures with 6, 12, and 25 nm collector variations and a triple barrier structure (TBRTS).

III. Simulation and Structure Design Details

The simulations were performed using the WinGreen simulation package [25], which is based on a nonequilibrium Green's

TABLE I
WINGREEN INPUT PARAMETERS FOR THE DOUBLE BARRIER RESONANT TUNNELING STRUCTURE WITH A 12 nm SPACER REPORTED BY KANAYA *et al.* [13]

Thickness (nm)[a]	Material	Scattering parameter	N-Type doping (10^{16} cm^{-3})	Doping energy level (eV)[b]
30	$In_{0.53}Ga_{0.47}As$	0.0600	5000	0.005
5	$In_{0.53}Al_{0.10}Ga_{0.37}As$	0.0600	5000	0.005
20	$In_{0.53}Al_{0.10}Ga_{0.37}As$	0.0450	300	0.005
2	$In_{0.53}Al_{0.10}Ga_{0.37}As$	0.0034	0.01	0.005
M3	AlAs	0.0034	0.01	0.005
M11	$In_{0.90}Ga_{0.10}As$	0.0034	0.01	0.005
M3	AlAs	0.0034	0.01	0.005
12	$In_{0.53}Ga_{0.47}As$	0.0034	0.01	0.005
15	$In_{0.53}Ga_{0.47}As$	0.0600	5000	0.005

These parameters are used throughout the simulations presented, with only the layer thickness and layer material being altered.
[a] or monolayers (ML), denoted by the prefix "M.'.
[b] relative to the conduction band minimum.

function approach to quantum transport in laterally extended layered heterostructures.

Material layer properties such as electron effective mass, dielectric constant, bandgap energy, and valence band offsets are defined in a material database, extracted from [26]–[29], which were modified to also take into account the effects of strain, where appropriate, and simulation temperature, which was maintained at 300 K .

To qualify the simulations and ensure that the theoretical results were comparable to experimental devices, double barrier structures reported by Kanaya *et al.* [13] and a triple barrier structure reported by Sekiguchi *et al.* [30] were simulated. The scattering parameter, which describes elastic scattering mechanisms such as phonon, impurity, and interface roughness, is implemented in a single optical potential function as an imaginary self-energy for the Green's functions. This value was fine tuned for both double and triple barrier structures by comparison of the theoretical and experimental *I–V* characteristics, which show good agreement, and are shown in Fig. 1. The substructure observed in the negative differential conductance region of the experimental traces in Fig. 1 is associated with the time-averaged measurement of high-frequency oscillations caused by instabilities in the measurement circuit. These features are not present in the simulated data, which considers only the steady-state solutions. The input parameters for the simulated Kanaya *et al.* double barrier structure with a 12 nm spacer are given in Table I and these parameters form the basis for the simulations presently reported, with only the layer thickness, or layer material varied.

Previous studies of triple barrier resonant tunneling structures have shown that significant charge accumulation can occur in the quantum wells of the structure [31], which is a problem for high-frequency applications due to the increased device capacitance. As a result, careful consideration and design of the triple barrier structure is required to minimize any potential charge accumulation.

To a first approximation, charge accumulation in these structures can be minimized by ensuring that

$$B_E \geq B_M + B_C \tag{8}$$

TABLE II
WIDTHS OF THE ACTIVE REGION LAYERS FOR THE SIMULATED TRIPLE BARRIER RTDS

Design	B_E (ML)	W_E (ML)	B_M (ML)	W_C (ML)	B_C (ML)
In53A	4	11	2	Varied	2
In53B	3	10	2	Varied	2
In53C	3	9	2	Varied	2
In53X	3	13	2	Varied	2

All structures utilize AlAs barriers and an $In_{0.53}Ga_{0.47}As$ collector quantum well, with an emitter quantum well alloy composition, $In_{0.90}Ga_{0.10}As$ for designs In53A, In53B, and In53C and $In_{0.80}Ga_{0.20}As$ for In53X.

where B_E, B_M, and B_C are the layer widths for the emitter, middle, and collector barriers, respectively. As the electron transmission probability crudely depends on the barrier widths, this imposes limits on the structure such that the transmission probability into the emitter quantum well is less than the transmission probability out of the emitter well, thus minimizing charge accumulation.

However, in reality, at energies equal to carriers in the three-dimensional (3-D) emitter and with bias across the structure

$$T_E > T_M > T_C \tag{9}$$

where T_E, T_M, and T_C are the transmission probability for the emitter, middle, and collector barriers, respectively. Thus, provided that (9) is still true at resonance, barrier width combinations such as 3 monolayers (ML), 2 ML, and 2 ML for the emitter, middle, and collector barriers, respectively, will allow for minimized charge accumulation.

IV. SIMULATION RESULTS AND DISCUSSION

The structure designs for those simulated are given in Table II, where the requirements for minimizing charge accumulation and thin barriers for high current density with fast tunneling times have been imposed. The potential barrier material has been chosen as aluminum arsenide (AlAs) to maximize the height of the confining potential barriers compared to the indium gallium arsenide composition ($In_xGa_{1-x}As$) of the emitter quantum well (W_E). The width of the collector quantum well

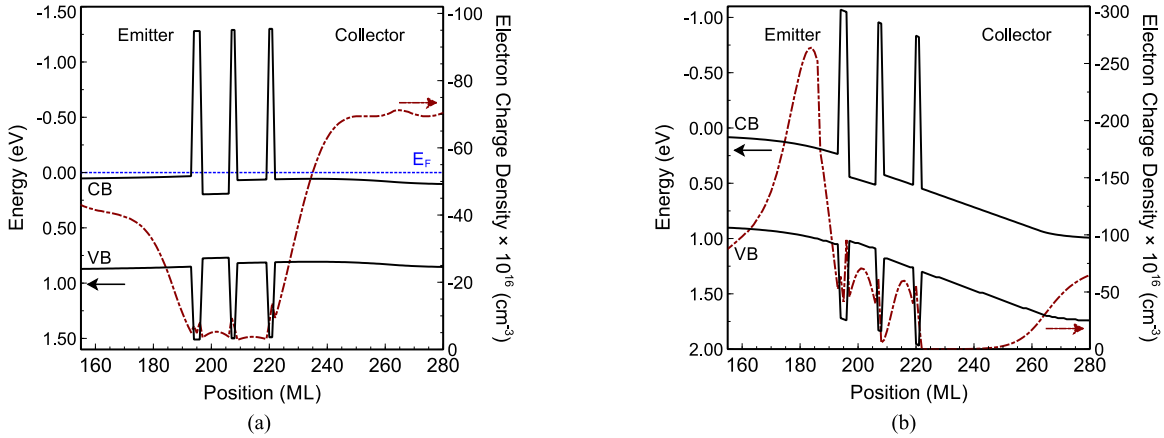

Fig. 2. (a) Zero bias (0.0 V) conduction and valence band potential profiles for the In53B design (black solid lines). The Fermi level at 0.00 eV is also shown (dashed blue line) along with the electron charge density (red dashed–dotted line). (b) The conduction and valence band potential profiles and electron charge density at 0.90 V for the In53B design.

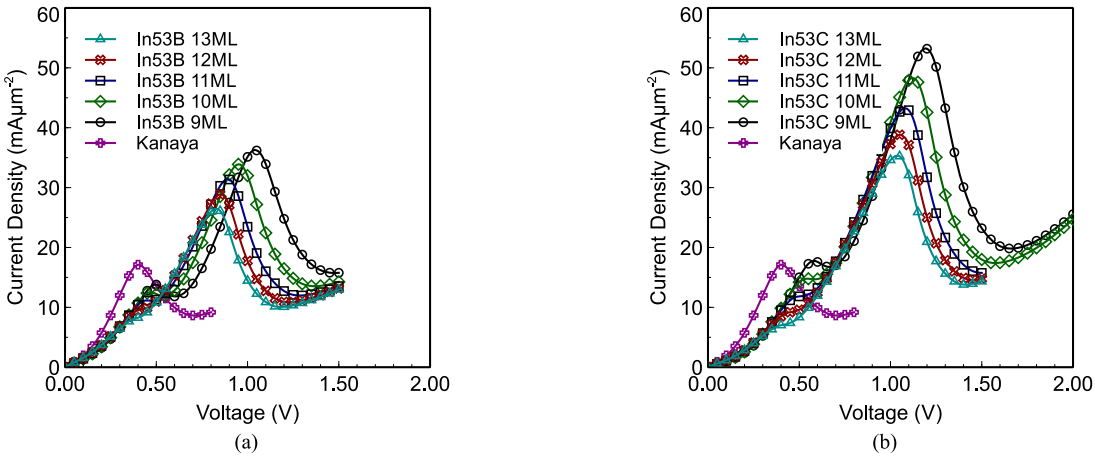

Fig. 3. Simulated current density–voltage characteristics for a selection of structures based on the (a) In53B and (b) In53C designs (Table II) with varying collector quantum well width. The characteristics for different monolayers collector well widths are shown in comparison to the double barrier structure by Kanaya *et al.* [13].

has been chosen to result in an active region, which is as close to being strain compensated as possible, where the strain introduced by the AlAs (tensile) and $In_xGa_{1-x}As$ (compressive for $x > 0.53$) layers has been approximately balanced when compared to the $In_{0.53}Ga_{0.47}As$ collector and emitter regions of the device, which are lattice matched to InP. The width of the collector quantum well (W_C) is optimized whilst the well alloy composition remains fixed at $In_{0.47}Ga_{0.53}As$.

The conduction and valence band potential profiles and electron charge density for the In53B design active region are shown in Fig. 2 at 0.0 V [see Fig. 2(a)] and at 0.90 V [see Fig. 2(b)], where the largest current resonance in this structure is observed. The electron charge distribution, shown in Fig. 2(b), indicates that there is minimal charge accumulation in the emitter quantum well in this structure, and is comparable to the simulated electron charge distribution for the Kanaya *et al.* double barrier structure (not shown).

Examples of the forward bias simulated current density–voltage characteristics are shown in Fig. 3(a) and (b). Due to the thin middle barrier in the triple barrier heterostructure design there is a large energy splitting between the quasi-confined quantum well 2-D electron states, and as such the transmission probability of electrons at these energies is very high. This results in an *I–V* characteristic in which two resonant peaks are present, as can be seen in Fig. 3(a) and (b).

The magnitude of the first and second observable resonant current peaks varies with collector quantum well width, as well as between different structure designs (In53A, In53B, In53C, and In53X). For high-frequency applications the largest resonant feature of the current density–voltage characteristics for the structure designs previously described were analyzed to extract important measures such as an average negative differential conductance (G), steady-state output power density (P_{MAX}), output to input power ratio, and resonance peak voltage, where plots of these, for the variations of the structures described, are shown in Fig. 4(a) and (b) and Fig. 5(a) and (b).

With a low output to input power density ratio, increased negative differential conductance, and output power density, the

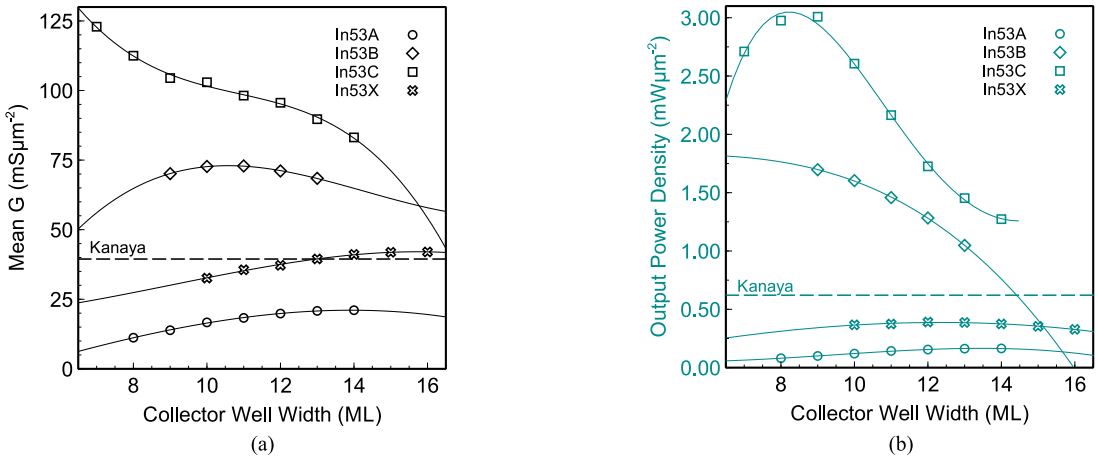

Fig. 4. (a) Calculated mean negative differential conductance G and (b) calculated steady-state output power density; plotted against the varied width of the collector quantum well for the In53A (open circles), In53B (open diamonds), In53C (open squares), and In53X (open crosses) variations given in Table II. Third-order polynomial fits are also shown, whereas the dashed lines represent the calculated values for the Kanaya *et al.* [13] double barrier structure with a 12 nm spacer.

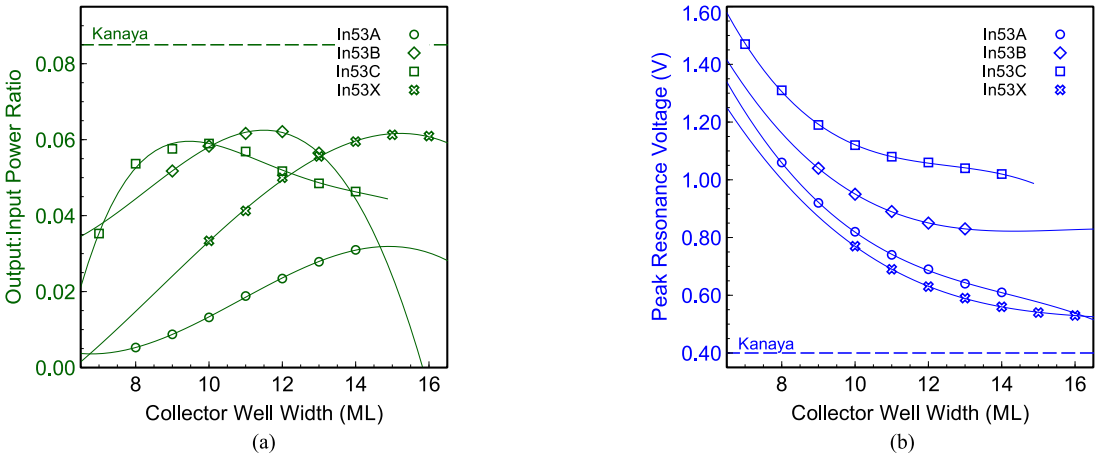

Fig. 5. (a) Calculated input to output power efficiency and (b) extracted resonance peak voltage; plotted against the varied width of the collector quantum well for the In53A (open circles), In53B (open diamonds), In53C (open squares), and In53X (open crosses) variations given in Table II. Third-order polynomial fits are also shown, whereas the dashed lines represent the calculated values for the Kanaya *et al.* [13] double barrier structure with a 12 nm spacer.

In53A structures perform poorly in comparison to the optimized double barrier structure by Kanaya *et al.*, as well as the In53B, In53C, and In53X triple barrier structure designs. This poor performance can be attributed to the thicker, 4 ML emitter barrier width and further emphasizes the need for thin barriers in these structures.

The In53B set of designs, however, are much more promising, with nearly double the negative differential conductance and output power density than that of the optimized double barrier structure. The resonances in these structures occur at higher voltages and, as such, despite In53B 11 ML and In53B 12 ML designs having the highest output power to input power density ratio, these values are still of lower efficiency than the optimized double barrier structure.

The series of In53C designs are very interesting structures, with resonances that occur at high voltages, but with extremely large ΔI and ΔV thus resulting in large output power density and negative differential conductance. These designs also appear to be relatively efficient with output to input power density ratios between ≈4% and 6%, due to the large peak resonance current in comparison to the off-resonant current. However, these structures pose a higher degree of uncertainty in the calculated values due to the high voltages at which the resonances occur. At such high voltages there are many more leakage mechanisms, which can contribute to the off-resonant current, which these simulations do not consider. As such the series of In53C designs must be treated with some caution.

The final set of designs, In53X that utilize an $In_{0.80}Ga_{0.20}As$ emitter quantum well rather than $In_{0.90}Ga_{0.10}As$, offer the lowest resonance peak voltages of all of the triple barrier structure designs. However, despite good efficiency with the wider collector quantum wells (15 and 16 ML) and negative differential conductances similar to the double barrier structure, the output power density for these structures is low and as such these structures overall perform quite poorly.

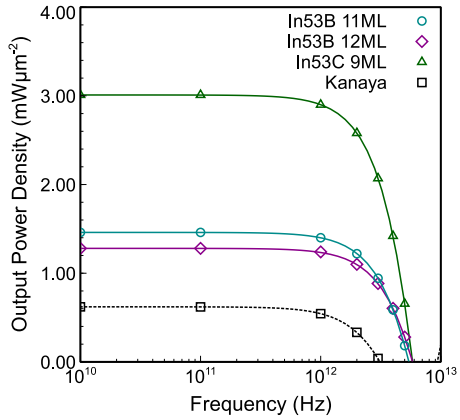

Fig. 6. Frequency-dependent output power density for a selection of the structures simulated. It can be seen there is a remarkable increase in both output power density and ultimate oscillation frequency in comparison to the optimized double barrier structure with a 12 nm spacer by Kanaya *et al.* [13].

From this analysis it is trivial to see that optimizing a structure, which improves upon all of the parameters considered here is not possible, as each design has some improvements, but sacrifices other aspects in order to achieve these benefits. Thus, the design of the structures should be tailored to the application, rather than using a simple superior design. For example, the series of In53C designs are likely to have superior output power density and negative conductance but become less efficient as a result.

To compare the frequency-dependent power of these simulated structures against the optimized double barrier structure, the tunneling time through the RTD (τ_{rtd}) has been calculated from the full width half-maximum of the transmission coefficient for the In53B 11 ML, In53B 12 ML, and In53C 9 ML structures and found to be 16 fs, 13 fs, and 13 fs, respectively. The transit time through the collector depletion region (τ_{dep}) is assumed to be equal to that calculated by Kanaya *et al.* [13], which is 60 fs. Therefore, from (7), the total delays of the charge carriers traveling through the structure (τ_T) are found to be 46 fs, 43 fs, and 43 fs for designs In53B 11 ML, In53B 12 ML, and In53C 9 ML, respectively. The intrinsic response frequency limit (f_{c}) due to the tunneling and transit times through the structure can be calculated from [20]

$$f_{\text{c}} = \frac{1}{2(2\tau_{\text{rtd}} + \tau_{\text{dep}})} \tag{10}$$

and are found to be ≈5.43 THz, ≈5.81 THz, and ≈5.81 THz for designs In53B 11 ML, In53B 12 ML, and In53C 9 ML, respectively. The calculated frequency-dependent power density for these designs, from (6), along with the optimized double barrier structure by Kanaya *et al.* [13] are shown in Fig. 6.

There is a clear improvement in the output power density in the THz region with the maximum frequency of oscillation also increased due to the reduction in the total transit time through the structure. This is a very important result as these increases significantly improve the output power density at frequencies between approximately 2 and 5 THz, and as such increase the practicality for applications of room temperature RTD devices in this frequency range.

To assess the potential suitability of real-world structures realizable with current basic fabrication technologies, the maximum oscillation frequencies of typical 1 μm^2 mesa devices are calculated using (3). Literature values for R_{S} and C_{D} have been used. R_{S} that includes contact resistance, spreading resistance, and bulk resistance is assumed to be 0.247 $\Omega\mu$m^{-2} from [32] and $C_{\text{D}}(= C_{\text{dep}} + C_{\text{rtd}} + C_{\text{c}})$ has been calculated. The capacitance associated with the device depletion region (C_{dep}) is assumed to be 6 fFμm^{-2} for a 12 nm spacer layer (taken from [13]), with the contact capacitance (C_{c}) assumed to be 14 fFμm^{-2} from similarly reported structures [32]. Additional capacitance due to the tunneling and transit delay of carriers for the small-signal case and in the low frequency regime ($\tau_{\text{dep}}\omega$, $\tau_{\text{rtd}}\omega \ll 1$) can be given by [20]

$$C_{\text{rtd}} \simeq \left(\tau_{\text{rtd}} + \frac{\tau_{\text{dep}}}{2}\right) G \tag{11}$$

which, for these structures, can be assumed to be ≈5 fFμm^{-2}. Estimates of the maximum frequencies for a 1 μm^2 device for designs In53B 11 ML, In53B 12 ML, and In53C 9 ML, with negative differential conductance values G of 72.9 mSμm^{-2}, 72.8 mSμm^{-2}, and 104.4 mSμm^{-2} are found to be ≈3.4 THz, ≈3.4 THz, and ≈4.0 THz, respectively.

However, at these predicted high frequencies, the low frequency regime assumption made in (11) is not valid, and thus the full frequency dependence of both C_{rtd} and the negative differential conductance must be considered [20]

$$C_{\text{rtd}}(\omega) = \frac{2\sin\left[\omega\left(\tau_{\text{rtd}} + \frac{\tau_{\text{dep}}}{2}\right)\right]\sin\frac{\omega\tau_{\text{dep}}}{2}}{\omega^2\tau_{\text{dep}}} G(\omega) \tag{12}$$

$$G(\omega) = \frac{2\cos\left[\omega\left(\tau_{\text{rtd}} + \frac{\tau_{\text{dep}}}{2}\right)\right]\sin\frac{\omega\tau_{\text{dep}}}{2}}{\omega\tau_{\text{dep}}} G. \tag{13}$$

Solving (3), (12), and (13) iteratively to a converged solution results in revised f_{MAX} values of ≈3.1 THz, ≈3.1 THz, and ≈3.4 THz for 1 μm^2 mesa devices of structure designs In53B 11 ML, In53B 12 ML, and In53C 9 ML, respectively.

By further decreasing the mesa size, the reduction in device capacitance results in an increased f_{MAX}, but a decrease in the absolute output power of the device. Thus, the tradeoff between frequency and output power still applies here, and the device design must be tailored to the application. However, these structures show considerable promise for practical applications in the THz frequency range.

It is also likely that the triple barrier structures can be further optimized to increase device efficiency by altering the 3-D emitter region alloy composition such that the resonances occur at lower voltages. Further performance optimization can also be carried out by altering the barrier and well compositions, as well as a reoptimization of the collector spacer considering the tradeoff between the device capacitance and collector depletion region transit time, similar to that carried out by Kanaya *et al.* [13].

In reality, however, the large-scale, low-cost, high-volume manufacturing of these structures still remains extremely challenging due to the complex engineering of the associated circuit required for such RTD devices and the precise epitaxial growth of such thin layers. The variability of the tunneling current for proposed electronic devices has been previously explored [33] and is still applicable today. Although research devices with a low yield are likely possible, a single monolayer variation in the emitter barrier can result in a significant change in the *I–V* characteristic and so result in a dramatically different device response. Therefore, any attempt to scale such devices to low cost manufacturable yields will still require significant work on the control of epitaxy and fabrication processes.

V. Conclusion

We have designed, simulated, and optimized a series of strain compensated InGaAs/AlAs triple barrier resonant tunneling heterostructures. The use of a triple barrier structure active region improves both output power density $\approx 3\ \mathrm{mW}\mu\mathrm{m}^{-2}$ at 1 THz and maximum output frequency ≥ 4 THz in comparison to state-of-the-art double barrier structures. However, growth and fabrication of devices based on these structures still remains extremely challenging due to the complexity of the circuitry required and precise epitaxial growth of such thin layers.

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